Md Zesun Ahmed Mia

Process Integration Engineer | Semiconductor Fabrication & Yield

Process integration engineer with extensive hands-on experience in semiconductor fabrication. Expertise in developing, optimizing, and troubleshooting process flows for novel devices.

Education

08/2022–Present **Ph.D. in Electrical Engineering**, *Pennsylvania State University*, University Park, PA, USA, *CGPA: 4.00/4.00* | Advisor: Dr. Abhronil Sengupta | Expected Graduation: 05/2027

08/2022–08/2024 **M.S. in Electrical Engineering**, *Pennsylvania State University*, University Park, PA, USA, *CGPA: 4.00/4.00* | Thesis: Neuromorphic Computing for Lifelong Learning

02/2015–04/2019 **B.Sc. in Electrical and Electronic Engineering**, *Bangladesh University of Engineering & Technology (BUET)*, Dhaka, Bangladesh, *CGPA: 3.81/4.00*

Academic Research and Teaching Experience

08/2022–Present **Graduate Research Assistant**, *Penn State*, University Park, PA

- Developed and documented a complete fabrication recipe for spintronic Hall bar devices, managing process steps from lithography to deposition in a university cleanroom.
- Utilized TCAD simulations to model the impact of process variations on FET device physics, providing critical feedback for process development.
- Bridged process development and system design by establishing a workflow to assess how fabrication choices affect hardware-aware ML model performance.

08/2024–05/2025 **Graduate Teaching Assistant**, *Penn State*, State College, PA

- Taught Cadence Virtuoso (schematic/layout), PDK usage, DRC/LVS, and analog/digital design flows; created hands-on lab modules and guided tool/debug workflows.
- Supervised Capstone projects for 90+ undergraduate students across communications, electronics, and firmware: supported Raspberry Pi/Arduino development, software-defined radio experiments, PCB design, and system integration end-to-end.

02/2021–08/2022 **Lecturer**, *University of Liberal Arts Bangladesh (ULAB)*, Dhaka, Bangladesh

- Taught undergraduate courses: Solid State Devices, Digital Circuit Design, Semiconductor Device Physics.
- Developed lab modules and supervised projects on semiconductor devices and circuits.

Technical Skills

Process Integration & Fabrication	Semiconductor process integration, thin film deposition (CVD, HDP-CVD, PVD), etching, lithography, wet bench, process-device co-design, yield optimization, scalable manufacturing, memory device fabrication, process optimization for memory devices, Process control (SPC, process monitoring), NVM device integration for Compute-in-Memory
Modeling & Reliability	Device modeling (Compact modeling, SPICE modeling, behavioral modeling), TCAD, parameter extraction, Verilog-A, reliability testing, retention analysis
Characterization	Ellipsometer, profilometer, SEM, AFM, electrical testing, oscilloscope, signal generator, magnetic probe station, Metrology (XRR, XRD, ellipsometry, profilometry), device-level energy/latency characterization for in-memory compute
Programming	Python, CUDA, MATLAB, Verilog, C/C++, Bash, Linux/Unix
EDA/Simulation	Cadence Virtuoso, Spectre, HSPICE, COMSOL, ModelSim, Synopsys (Design Compiler, PrimeTime, VCS), CIM (Compute-In-Memory) Systems
ML/AI Tools	PyTorch, TensorFlow, TensorRT, Data Visualization (Matplotlib, Seaborn, Plotly), Pandas, NumPy, JMP, Jupyter, LaTeX, AI accelerator development, Systolic Arrays, HPC applications, parallel computing architectures
Collaboration	Git, Microsoft Office, Google Workspace
AI Dev.	Generative and agentic AI tools (Cursor, Copilot, etc.) for research, design, and code development

Industrial Experience

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in zesun-ahmed • zesun33

05/2026–07/2026 **Machine Learning Engineer Intern**, *Micron Technology*, Richardson, TX

- Model Non-Volatile Memory (NVM) device characteristics (technology-agnostic) to evaluate speedup and energy savings for memory-centric ML inference.
- Characterize LLM serving performance (TPOT, TTFT) under Prefill-Decode and Attention-FFN disaggregation schemes (PD, AFD) for hyperscale inference deployment.
- Investigate quantization error and CIM analog error mitigation techniques to preserve model accuracy under analog compute noise and limited ADC precision.

05/2025–07/2025 **Graduate Technical Intern**, *Intel Corporation*, Hillsboro, OR

- Designed comprehensive Design of Experiments (DOE) for thin film deposition process optimization supporting high-volume semiconductor manufacturing.
- Investigated novel process integration tools for next-generation manufacturing, focusing on process window optimization and yield improvement.
- Conducted extensive process characterization using AFM, DSIMS, FTIR, XRR, TDS, and stress analysis for process control and validation.
- Implemented AI-powered predictive models for automated process recipe optimization and real-time process monitoring in manufacturing environment.
- Developed statistical analysis frameworks to assess process variability and establish robust process control limits for production scalability.

Projects

Spintronic Device-Based Memory Lead Student Researcher, 2023–Present. Led end-to-end fabrication of spintronic memory arrays using e-beam lithography, sputtering deposition, and lift-off patterning. Performed comprehensive electrical characterization (I-V, R-H loops, retention, endurance) and extracted device parameters for compact model development. Advanced non-volatile memory technologies for neuromorphic computing and in-memory processing applications.

FeFET Device Physics & Modeling Lead Student Researcher, 2022–Present. Designed and simulated advanced FET architectures using TCAD (Silvaco/Sentaurus) and developed physics-based models for FeFETs in MATLAB. Utilized experimental characterization data of Ferroic devices to extract switching characteristics, retention, and device parameters for algorithm-hardware co-design and next-generation memory applications.

Astromorphic Transformer Lead Student Researcher, 2022–2025. Developed a bioplausible transformer architecture leveraging neuron-astrocyte interactions to emulate self-attention mechanisms. Incorporated Hebbian and presynaptic plasticities with non-linearities and feedback, achieving superior accuracy and faster convergence on sentiment classification (IMDB), image classification (CIFAR-10), and language modeling (WikiText-2) tasks. See publication: [IEEE TCDS 2025].

Select Publications

[1] **Md Zesun Ahmed Mia**, Jiahui Duan, Kai Ni, and Abhronil Sengupta. "Trilinear Compute-in-Memory Architecture for Energy-Efficient Transformer Acceleration". In: *arXiv preprint arXiv:2604.07628* (2026).

[2] **Md Zesun Ahmed Mia**, Malyaban Bal, and Abhronil Sengupta. "Delving deeper into astromorphic transformers". In: *IEEE Transactions on Cognitive and Developmental Systems* (2025).

[3] Tao Zhang, Mingjie Hu, **Md Zesun Ahmed Mia**, Hao Zhang, Wei Mao, Katsuyuki Fukutani, Hiroyuki Matsuzaki, Lingzhi Wen, Cong Wang, Hongbo Zhao, et al. "Self-sensitizable neuromorphic device based on adaptive hydrogen gradient". In: *Matter* 7.5 (2024), pp. 1799–1816.

[4] KM Ashraful Hoque Fahim, Md Jubair Hasan Khalid, **Md Zesun Ahmed Mia**, and Mirza Rasheduzzaman. "Study of 3-nm Cylindrical GAAFETs with Variations in High-k Dielectric Gate-oxide Materials". In: *2022 IEEE Symposium on Industrial Electronics & Applications (ISIEA)*. IEEE. 2022, pp. 1–5.

Recognitions

- Melvin P. Bloom Memorial Outstanding Doctoral Research Award (2026)
- The Wormley Family Graduate Fellowship, Harry G. Miller Fellowships in Engineering (2025)
- Arthur Waynick Graduate Scholarship (2024),Milton and Albertha Langdon Memorial Fellowship (2023), Melvin P. Bloom Memorial Fellowship (2022)

Professional Affiliations

- Reviewer, NeurIPS (2026), IOP Physica Scripta (2026), IEEE MWSCAS (2026)
- Reviewer, IEEE TNNLS (2025), Design Automation Conference (DAC) (2025), IEEE MWSCAS (2025)
- Student Member, IEEE (2015-Present), Executive Member, EDS, IEEE BD (2021-2022)

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