Md Zesun Ahmed Mia

Process Integration Engineer | Semiconductor Fabrication & Yield

Process integration engineer with extensive hands-on experience in semiconductor fabrication. Expertise in developing, optimizing, and troubleshooting process flows for novel devices.

Education

08/2022–08/2027 (Expected) **Ph.D. in Electrical Engineering**, *Pennsylvania State University*, University Park, PA, USA, *CGPA: 4.00/4.00*
Advisor: Dr. Abhronil Sengupta

08/2022–08/2024 **M.S. in Electrical Engineering**, *Pennsylvania State University*, University Park, PA, USA, *CGPA: 4.00/4.00*
Thesis: Neuromorphic Computing for Lifelong Learning

02/2015–04/2019 **B.Sc. in Electrical and Electronic Engineering**, *Bangladesh University of Engineering & Technology (BUET)*, Dhaka, Bangladesh, *CGPA: 3.81/4.00*

Industrial Experience

05/2025–07/2025 **Graduate Technical Intern**, *Intel Corporation*, Hillsboro, OR

- Designed comprehensive Design of Experiments (DOE) for thin film deposition process optimization supporting high-volume semiconductor manufacturing.
- Investigated novel process integration tools for next-generation manufacturing, focusing on process window optimization and yield improvement.
- Conducted extensive process characterization using AFM, DSIMS, FTIR, XRR, TDS, and stress analysis for process control and validation.
- Implemented AI-powered predictive models for automated process recipe optimization and real-time process monitoring in manufacturing environment.
- Developed statistical analysis frameworks to assess process variability and establish robust process control limits for production scalability.

09/2020–07/2021 **R&D Engineer**, *SEMWAVES Ltd.*, London, UK, part-time

- Delivered a 50 kW hybrid renewable system (solar + smallscale hydro) for an offgrid Bangladeshi site, supporting reliable community power.
- Owned technical leadership and coordination (vendors, field teams, stakeholders); directed device selection, integration, QA/safety procedures, and optimization against load profiles and uptime targets.

Technical Skills

Process Integration & Fabrication	Semiconductor process integration, thin film deposition (CVD, HDP-CVD, PVD), etching, lithography, wet bench, process-device co-design, yield optimization, scalable manufacturing, memory device fabrication, process optimization for memory devices, Process control (SPC, process monitoring, yield enhancement)
Modeling & Reliability	Device modeling (Compact modeling, SPICE modeling, behavioral modeling), TCAD, parameter extraction, Verilog-A, reliability testing, retention analysis
Characterization	Ellipsometer, profilometer, SEM, AFM, electrical testing, oscilloscope, signal generator, magnetic probe station, Metrology (XRR, XRD, ellipsometry, profilometry)
Programming	Python, MATLAB, Verilog, C/C++, Bash, Linux/Unix
EDA/Simulation	Cadence Virtuoso, Spectre, HSPICE, COMSOL, ModelSim, Synopsys (Design Compiler, PrimeTime, VCS), CIM (Compute-In-Memory) Systems
ML/AI Tools	PyTorch, TensorFlow, Data Visualization (Matplotlib, Seaborn, Plotly), Pandas, NumPy, JMP, Jupyter, LaTeX, AI accelerator development, HPC applications, parallel computing architectures
Collaboration	Git, Slack, Microsoft Office, Google Workspace

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in zesun-ahmed • zesun33

AI-Assisted Development: Advanced use of generative and agentic AI tools (Cursor, Copilot, VSCode, ChatGPT Agents) for research, design, and code development

Academic Research and Teaching Experience

08/2022–Present **Graduate Research Assistant**, *Penn State*, University Park, PA
- Developed and documented a complete fabrication recipe for spintronic Hall bar devices, managing process steps from lithography to deposition in a university cleanroom.
- Utilized TCAD simulations to model the impact of process variations on FET device physics, providing critical feedback for process development.
- Bridged process development and system design by establishing a workflow to assess how fabrication choices affect hardware-aware ML model performance.

08/2024–05/2025 **Graduate Teaching Assistant**, *Penn State*, State College, PA
- Taught Cadence Virtuoso (schematic/layout), PDK usage, DRC/LVS, and analog/digital design flows; created hands-on lab modules and guided tool/debug workflows.
- Supervised Capstone projects for 90+ undergraduate students across communications, electronics, and firmware: supported Raspberry Pi/Arduino development, software-defined radio experiments, PCB design, and system integration end-to-end.

02/2021–08/2022 **Lecturer**, *University of Liberal Arts Bangladesh (ULAB)*, Dhaka, Bangladesh
- Taught undergraduate courses: Solid State Devices, Digital Circuit Design, Semiconductor Device Physics, Power Electronics.
- Developed lab modules and supervised projects on semiconductor devices and circuits.

Projects

Astromorphic Transformer: Lead Student Researcher, 2022–2025. Developed a bioplausible transformer architecture that uses neuron-astrocyte interactions to emulate self-attention mechanisms. Incorporated Hebbian and presynaptic plasticities with non-linearities and feedback, achieving improved accuracy and learning speed on sentiment classification, image classification, and language modeling tasks. See publication: [IEEE TCDS].

Spintronic Device-Based Memory: Lead Student Researcher, 2023–Present. Led the fabrication and comprehensive characterization of spintronic memory arrays for machine learning systems, advancing non-volatile memory technologies to enhance computational performance.

Select Publications

[1] Md Zesun Ahmed Mia, Malyaban Bal, and Abhronil Sengupta. "Delving deeper into astromorphic transformers". In: *IEEE Transactions on Cognitive and Developmental Systems* (2025).

[2] Md Zesun Ahmed Mia et al. "Impact of Doping and Defects on Thermal Transport of Monolayer GaN Nanoribbons: A Molecular Dynamics Simulation Study". In: *2024 13th International Conference on Electrical and Computer Engineering (ICECE)*. IEEE. 2024, pp. 685–690.

[3] Tao Zhang et al. "Self-sensitizable neuromorphic device based on adaptive hydrogen gradient". In: *Matter* 7.5 (2024), pp. 1799–1816.

[4] KM Ashraful Hoque Fahim et al. "Study of 3-nm Cylindrical GAAFETs with Variations in High-k Dielectric Gate-oxide Materials". In: *2022 IEEE Symposium on Industrial Electronics & Applications (ISIEA)*. IEEE. 2022, pp. 1–5.

Recognitions

- The Wormley Family Graduate Fellowship, Harry G. Miller Fellowships in Engineering (2025)
- Arthur Waynick Graduate Scholarship (2024)
- Milton and Albertha Langdon Memorial Fellowship (2023)
- Melvin P. Bloom Memorial Fellowship (2022)

Professional Affiliations

- Reviewer, Design Automation Conference (DAC) 2025, IEEE MWSCAS 2025, IACCESS 2024
- Student Member, IEEE (2015-Present), Executive Member, EDS, IEEE BD (2021-2022)

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