Md Zesun Ahmed Mia

Hardware Engineer | ML-Hardware Co-Design & AI Acceleration

Research engineer specializing in the co-design of machine learning algorithms and hardware accelerators. Expertise in device-circuit-ML integration and hands-on hardware prototyping.

Education

08/2022–08/2027 (Expected) **Ph.D. in Electrical Engineering**, *Pennsylvania State University*, University Park, PA, USA, *CGPA: 4.00/4.00*
Advisor: Dr. Abhronil Sengupta

08/2022–08/2024 **M.S. in Electrical Engineering**, *Pennsylvania State University*, University Park, PA, USA, *CGPA: 4.00/4.00*
Thesis: Neuromorphic Computing for Lifelong Learning

02/2015–04/2019 **B.Sc. in Electrical and Electronic Engineering**, *Bangladesh University of Engineering & Technology (BUET)*, Dhaka, Bangladesh, *CGPA: 3.81/4.00*

Industrial Experience

05/2025–07/2025 **Graduate Technical Intern**, *Intel Corporation*, Hillsboro, OR
- Developed AI-driven models for process-circuit co-optimization in ML accelerator hardware, focusing on yield prediction and performance enhancement.
- Applied machine learning to optimize thin film deposition parameters affecting AI hardware circuit characteristics and system performance.
- Utilized statistical analysis (JMP) and AI models to predict process impact on circuit electrical parameters and device reliability for ML hardware.

09/2020–07/2021 **R&D Engineer**, *SEMWAVES Ltd.*, London, UK, part-time
- Delivered a 50 kW hybrid renewable system (solar + smallscale hydro) for an offgrid Bangladeshi site, supporting reliable community power.
- Owned technical leadership and coordination (vendors, field teams, stakeholders); directed device selection, integration, QA/safety procedures, and optimization against load profiles and uptime targets.

Technical Skills

ML Hardware	Neuromorphic hardware, ML accelerator/ASIC design, device-circuit-ML co-design, FPGA prototyping, Hardware-in-the-loop training, Quantization (PTQ/QAT), pruning, distillation, mixed-precision (FP16/INT8), graph optimization, hardware-aware training, Processing-in-Memory (PIM), near-memory computing, memory-centric computing, data flow optimization, HPC applications, parallel computing architectures
EDA/Sim.	Cadence Virtuoso, Spectre, HSPICE, TCAD, COMSOL, ModelSim (digital simulation), Quartus (FPGA development), Vivado, Synopsys (Design Compiler, PrimeTime, VCS), CIM (Compute-In-Memory) Systems
Programming	Python, MATLAB, Verilog, Shell, C/C++, Bash, Linux/Unix
ML/AI Tools	ONNX, TensorRT PyTorch, TensorFlow, Data Visualization (Matplotlib, Seaborn, Plotly), Pandas, NumPy, JMP, Jupyter, LaTeX, Weights & Biases
AI-Assisted Development	Advanced use of generative and agentic AI tools (Cursor, Copilot, VSCode, ChatGPT Agents) for research, design, and code development
Hardware	Device-circuit co-design, PCB design, Oscilloscope, Signal Generator, LabVIEW
Digital/ASIC	RTL, Synthesis, P&R, Verification, DFT, Timing Closure
Collaboration	Git, Slack, Microsoft Office, Google Workspace

Academic Research and Teaching Experience

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08/2022–Present **Graduate Research Assistant**, *Penn State*, University Park, PA
- Leading the development of an ML accelerator by creating a synergistic design flow that bridges Transformer algorithms with underlying hardware capabilities.
- Pioneered a system-level integration strategy for spintronic devices using hardware-aware training, demonstrating a clear path from device fabrication to system application.
- Researched brain-inspired ML systems, developing a novel Astromorphic Transformer that showed performance improvements over vanilla models.

08/2024–05/2025 **Graduate Teaching Assistant**, *Penn State*, State College, PA
- Taught Cadence Virtuoso (schematic/layout), PDK usage, DRC/LVS, and analog/digital design flows; created hands-on lab modules and guided tool/debug workflows.
- Supervised Capstone projects for 90+ undergraduate students across communications, electronics, and firmware: supported Raspberry Pi/Arduino development, software-defined radio experiments, PCB design, and system integration end-to-end.

02/2021–08/2022 **Lecturer**, *University of Liberal Arts Bangladesh (ULAB)*, Dhaka, Bangladesh
- Taught undergraduate courses: Solid State Devices, Digital Circuit Design, Semiconductor Device Physics, Power Electronics.
- Developed lab modules and supervised projects on semiconductor devices and circuits.

Research Projects

Astromorphic Transformer Lead Student Researcher, 2022–2025. Developed a bioplausible transformer architecture that uses neuron-astrocyte interactions to emulate self-attention mechanisms. Incorporated Hebbian and presynaptic plasticities with non-linearities and feedback, achieving improved accuracy and learning speed on sentiment classification, image classification, and language modeling tasks. See publication: [IEEE TCDS].

MIPS Microprocessor Design Lead Student Researcher, 2018–2019. Designed and implemented a 5-stage pipelined MIPS microprocessor in Verilog, supporting instruction/data memory, forwarding, and hazard detection. Verified functionality through simulation and synthesized for FPGA deployment.

Neuromorphic Cybersecurity Lead Student Researcher, 2023–2025. Developed a Hierarchical Dynamic Spiking Neural Network (D-SNN) for Network Intrusion Detection Systems (NIDS). The architecture employs a static SNN detector followed by an adaptive dynamic SNN classifier using GWR-inspired structural plasticity and a novel Adaptive STDP (Ad-STDP) learning rule. Demonstrated 85.3% overall accuracy on UNSW-NB15 benchmark in lifelong learning scenarios, mitigating catastrophic forgetting while adapting to new attack types. See publication: [arXiv], [ICONS 2025].

Select Publications

[1] Md Zesun Ahmed Mia, Malyaban Bal, and Abhronil Sengupta. "Delving deeper into astromorphic transformers". In: *IEEE Transactions on Cognitive and Developmental Systems* (2025).

[2] Md Zesun Ahmed Mia et al. "Neuromorphic Cybersecurity with Semi-supervised Lifelong Learning". In: *arXiv preprint arXiv:2508.04610* (2025).

[3] Md Zesun Ahmed Mia, Malyaban Bal, and Abhronil Sengupta. *RMAAT: A Bio-Inspired Approach for Efficient Long-Context Sequence Processing in Transformers*. 2024. URL: https://openreview.net/forum?id=ikSrEv8FId.

[4] Md Moinul Islam et al. "DCNN-LSTM based audio classification combining multiple feature engineering and data augmentation techniques". In: *Intelligent Computing & Optimization: Proceedings of the 4th International Conference on Intelligent Computing and Optimization 2021 (ICO2021) 3*. Springer. 2022, pp. 227–236.

Recognitions

- The Wormley Family Graduate Fellowship, Harry G. Miller Fellowships in Engineering (2025)
- Arthur Waynick Graduate Scholarship (2024)
- Milton and Albertha Langdon Memorial Fellowship (2023)
- Melvin P. Bloom Memorial Fellowship (2022)

Professional Affiliations

- Reviewer, Design Automation Conference (DAC) 2025, IEEE MWSCAS 2025, IACCESS 2024
- Student Member, IEEE (2015-Present), Executive Member, EDS, IEEE BD (2021-2022)

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