Md Zesun Ahmed Mia

Specialist in IC Design for Logic, Memory, & Mixed-Signal Systems

Expert in translating system requirements into robust IC designs for logic, memory, and mixed-signal applications. Adept at leveraging EDA tools for design, verification, and layout.

Education

08/2022–08/2027 (Expected) **Ph.D. in Electrical Engineering**, *Pennsylvania State University*, University Park, PA, USA, *CGPA: 4.00/4.00*
Advisor: Dr. Abhronil Sengupta

08/2022–08/2024 **M.S. in Electrical Engineering**, *Pennsylvania State University*, University Park, PA, USA, *CGPA: 4.00/4.00*
Thesis: Neuromorphic Computing for Lifelong Learning

02/2015–04/2019 **B.Sc. in Electrical and Electronic Engineering**, *Bangladesh University of Engineering & Technology (BUET)*, Dhaka, Bangladesh, *CGPA: 3.81/4.00*

Industrial Experience

05/2025–07/2025 **Graduate Technical Intern**, *Intel Corporation*, Hillsboro, OR
- Optimized thin film deposition processes affecting microprocessor circuit performance and electrical characteristics for advanced logic devices.
- Designed DOE to control critical dimensions (CD) impacting yield and electrical parameters in next-generation processors.
- Applied statistical modeling to predict process impact on circuit performance metrics and device reliability.

09/2020–07/2021 **R&D Engineer**, *SEMWAVES Ltd.*, London, UK, part-time
- Delivered a 50 kW hybrid renewable system (solar + smallscale hydro) for an offgrid Bangladeshi site, supporting reliable community power.
- Owned technical leadership and coordination (vendors, field teams, stakeholders); directed device selection, integration, QA/safety procedures, and optimization against load profiles and uptime targets.

Technical Skills

Digital/ASIC	RTL design and verification, Verilog/VHDL, Digital circuit simulation (Gate-level, RTL, transistor-level), FPGA prototyping, Synthesis, P&R, DFT, Static timing analysis, Timing closure, CMOS/FinFET circuit design, SRAM/DRAM design and optimization, Processing-in-Memory (PIM), memory controller design, VLSI/IC design, ASIC design flow, Digital logic design, Testbench development
EDA/Sim.	Cadence Virtuoso, Spectre, HSPICE, TCAD, COMSOL, ModelSim (digital simulation), Quartus (FPGA development), Vivado, Synopsys (Design Compiler, PrimeTime, VCS), CIM (Compute-In-Memory) Systems
Analog Des.	Op-amp and comparator design, Bandgap reference, Biasing circuits, Current mirrors, Differential pairs, Amplifiers, Filters, ADC/DAC, Noise analysis
Programming	Python, MATLAB, Verilog, Shell, C/C++, Bash, Linux/Unix
ML/AI Tools	PyTorch, TensorFlow, Data Visualization (Matplotlib, Seaborn, Plotly), Pandas, NumPy, JMP, Jupyter, LaTeX, AI accelerator development, HPC applications, parallel computing architectures
AI-Assisted Development	Advanced use of generative and agentic AI tools (Cursor, Copilot, VSCode, ChatGPT Agents) for research, design, and code development
Hardware	Device-circuit co-design, PCB design, Oscilloscope, Signal Generator, Spectrum Analyzer, LabVIEW, Circuit debugging and characterization
Collaboration	Git, Slack, Microsoft Office, Google Workspace

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Academic Research and Teaching Experience

08/2022–Present **Graduate Research Assistant**, *Penn State*, University Park, PA

- Engineered and validated compact models for emerging Ferroic devices (e.g. FeFETs) in MATLAB and Verilog-A for integration into standard cell and memory design workflows.
- Analyzed device-level characteristics of spintronic and FeFET devices to inform the design of robust, low-power logic and memory circuits.

08/2024–05/2025 **Graduate Teaching Assistant**, *Penn State*, State College, PA

- Taught Cadence Virtuoso (schematic/layout), PDK usage, DRC/LVS, and analog/digital design flows; created hands-on lab modules and guided tool/debug workflows.
- Supervised Capstone projects for 90+ undergraduate students across communications, electronics, and firmware: supported Raspberry Pi/Arduino development, software-defined radio experiments, PCB design, and system integration end-to-end.

02/2021–08/2022 **Lecturer**, *University of Liberal Arts Bangladesh (ULAB)*, Dhaka, Bangladesh

- Taught Digital Circuit Design including Verilog, logic synthesis, FPGA implementation.
- Developed hands-on lab modules for digital system design, RTL coding and verification.
- Supervised student projects on digital circuit implementation and FPGA prototyping.
- Taught undergraduate courses: Solid State Devices, Digital Circuit Design, Semiconductor Device Physics, Power Electronics.

Projects

MIPS Microprocessor Design — Lead Student Researcher, 2018–2019. Designed and implemented a 5-stage pipelined MIPS microprocessor in Verilog, supporting instruction/data memory, forwarding, and hazard detection. Verified functionality through simulation and synthesized for FPGA deployment.

Ultra Low Cost Electronic Braille Device — First Author, 2022–2024. Designed and implemented a solenoid-based electronic Braille device using 3D printing and Arduino microcontroller. The hexagonal-designed device weighs 338g, costs $20, employs PWM control for low power consumption, and connects via USB/Bluetooth to cellular devices and laptops. Achieved 100 frames/s refresh rate, enabling real-time text-to-braille translation for visually impaired users. See publication: [iCACCESS 2024].

Astromorphic Transformer — Lead Student Researcher, 2022–2025. Developed a bioplausible transformer architecture that uses neuron-astrocyte interactions to emulate self-attention mechanisms. Incorporated Hebbian and presynaptic plasticities with non-linearities and feedback, achieving improved accuracy and learning speed on sentiment classification, image classification, and language modeling tasks. See publication: [IEEE TCDS].

Select Publications

[1] Md Zesun Ahmed Mia, Malyaban Bal, and Abhronil Sengupta. "Delving deeper into astromorphic transformers". In: *IEEE Transactions on Cognitive and Developmental Systems* (2025).

[2] Md Zesun Ahmed Mia and Kazi Toukir Ahmed. "Ultra Low Cost, Low Power, High Speed Electronic Braille Device for Visually Impaired People". In: *2024 International Conference on Advances in Computing, Communication, Electrical, and Smart Systems (iCACCESS)*. IEEE. 2024, pp. 1–6.

[3] KM Ashraful Hoque Fahim et al. "Study of 3-nm Cylindrical GAAFETs with Variations in High-k Dielectric Gate-oxide Materials". In: *2022 IEEE Symposium on Industrial Electronics & Applications (ISIEA)*. IEEE. 2022, pp. 1–5.

Recognitions

- The Wormley Family Graduate Fellowship, Harry G. Miller Fellowships in Engineering (2025)
- Arthur Waynick Graduate Scholarship (2024)
- Milton and Albertha Langdon Memorial Fellowship (2023)
- Melvin P. Bloom Memorial Fellowship (2022)

Professional Affiliations

- Reviewer, Design Automation Conference (DAC) 2025, IEEE MWSCAS 2025, IACCESS 2024
- Student Member, IEEE (2015-Present), Executive Member, EDS, IEEE BD (2021-2022)

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