Md Zesun Ahmed Mia

Specialist in IC Design for Logic, Memory, & Mixed-Signal Systems

Expert in translating system requirements into robust IC designs for logic, memory, and mixed-signal applications. Adept at leveraging EDA tools for design, verification, and layout.

Education

08/2022–05/2027 (Expected) **Ph.D. in Electrical Engineering**, *Pennsylvania State University*, University Park, PA, USA, *CGPA: 4.00/4.00*
Advisor: Dr. Abhronil Sengupta

08/2022–08/2024 **M.S. in Electrical Engineering**, *Pennsylvania State University*, University Park, PA, USA, *CGPA: 4.00/4.00* | Thesis: Neuromorphic Computing for Lifelong Learning

02/2015–04/2019 **B.Sc. in Electrical and Electronic Engineering**, *Bangladesh University of Engineering & Technology (BUET)*, Dhaka, Bangladesh, *CGPA: 3.81/4.00*

Industrial Experience

05/2025–07/2025 **Graduate Technical Intern**, *Intel Corporation*, Hillsboro, OR
- Optimized thin film deposition processes affecting microprocessor circuit performance and electrical characteristics for advanced logic devices.
- Designed DOE to control critical dimensions (CD) impacting yield and electrical parameters in next-generation processors.
- Applied statistical modeling to predict process impact on circuit performance metrics and device reliability.

09/2020–07/2021 **R&D Engineer**, *SEMWAVES Ltd.*, London, UK, part-time
- Delivered a 50 kW hybrid renewable system (solar + smallscale hydro) for an offgrid Bangladeshi site, supporting reliable community power.
- Owned technical leadership and coordination (vendors, field teams, stakeholders); directed device selection, integration, QA/safety procedures, and optimization against load profiles and uptime targets.

Technical Skills

Digital/ASIC	RTL design and verification, Verilog/VHDL, Digital circuit simulation (Gate-level, RTL, transistor-level), FPGA prototyping, Synthesis, P&R, DFT, Static timing analysis, Timing closure, CMOS/FinFET circuit design, SRAM/DRAM design and optimization, SRAM circuit fundamentals, sense amplifier design, memory peripheral circuits, Systolic Arrays, PIM, memory controller design, VLSI/IC design, ASIC design flow, Digital logic design, Testbench development
EDA/Sim.	Cadence Virtuoso, Spectre, HSPICE, TCAD, COMSOL, ModelSim (digital simulation), Quartus (FPGA development), Vivado, Synopsys (Design Compiler, PrimeTime, VCS), CIM (Compute-In-Memory) Systems
Analog Des.	Op-amp and comparator design, Bandgap reference, Biasing circuits, Current mirrors, Differential pairs, Amplifiers, Filters, ADC/DAC, Noise analysis
Programming	Python, CUDA, MATLAB, Verilog, Shell, C/C++, Bash, Linux/Unix
ML/AI Tools	PyTorch, TensorFlow, TensorRT, Data Visualization (Matplotlib, Seaborn, Plotly), Pandas, NumPy, JMP, Jupyter, LaTeX, AI accelerator development, HPC applications, parallel computing architectures
AI Dev.	Generative and agentic AI tools (Cursor, Copilot, etc.) for research, design, and code development
Hardware	Device-circuit co-design, PCB design, Oscilloscope, Signal Generator, Spectrum Analyzer, LabVIEW, Circuit debugging and characterization
Collaboration	Git, Microsoft Office, Google Workspace

Academic Research and Teaching Experience

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08/2022–Present **Graduate Research Assistant**, *Penn State*, University Park, PA
- Engineered and validated compact models for emerging Ferroic devices (e.g. FeFETs) in MATLAB and Verilog-A for integration into standard cell and memory design workflows.
- Analyzed device-level characteristics of spintronic and FeFET devices to inform the design of robust, low-power logic and memory circuits.

08/2024–05/2025 **Graduate Teaching Assistant**, *Penn State*, State College, PA
- Taught Cadence Virtuoso (schematic/layout), PDK usage, DRC/LVS, and analog/digital design flows; created hands-on lab modules and guided tool/debug workflows.
- Supervised Capstone projects for 90+ undergraduate students across communications, electronics, and firmware: supported Raspberry Pi/Arduino development, software-defined radio experiments, PCB design, and system integration end-to-end.

02/2021–08/2022 **Lecturer**, *University of Liberal Arts Bangladesh (ULAB)*, Dhaka, Bangladesh
- Taught Digital Circuit Design including Verilog, logic synthesis, FPGA implementation.
- Developed hands-on lab modules for digital system design, RTL coding and verification.
- Supervised student projects on digital circuit implementation and FPGA prototyping.
- Taught undergraduate courses: Solid State Devices, Digital Circuit Design, Semiconductor Device Physics, Power Electronics.

Projects

Astromorphic Transformer Lead Student Researcher, 2022–2025. Developed a bioplausible transformer architecture leveraging neuron-astrocyte interactions to emulate self-attention mechanisms. Incorporated Hebbian and presynaptic plasticities with non-linearities and feedback, achieving superior accuracy and faster convergence on sentiment classification (IMDB), image classification (CIFAR-10), and language modeling (WikiText-2) tasks. See publication: [IEEE TCDS 2025].

Ultra Low Cost Electronic Braille Device First Author, 2022–2024. Designed and fabricated a portable, solenoid-based electronic Braille device using 3D printing and Arduino microcontroller. Achieved ultra-low cost ($20) and lightweight design (338g) with 100 frames/s refresh rate, enabling real-time text-to-braille translation. Implemented PWM control for low power consumption and USB/Bluetooth connectivity. See publication: [iCACCESS 2024].

MIPS Microprocessor Design Lead Student Researcher, 2018–2019. Designed and implemented a 5-stage pipelined MIPS microprocessor in Verilog with instruction/data memory, forwarding, and hazard detection. Verified functionality through comprehensive simulation and synthesized for FPGA deployment.

Select Publications

[1] **Md Zesun Ahmed Mia**, Jiahui Duan, Kai Ni, and Abhronil Sengupta. "Trilinear Compute-in-Memory Architecture for Energy-Efficient Transformer Acceleration". In: *arXiv preprint arXiv:2604.07628* (2026).

[2] **Md Zesun Ahmed Mia**, Malyaban Bal, and Abhronil Sengupta. "Delving deeper into astromorphic transformers". In: *IEEE Transactions on Cognitive and Developmental Systems* (2025).

[3] Arnob Saha, **Md Zesun Ahmed Mia**, Jiahui Duan, Kai Ni, and Abhronil Sengupta. "Toward Variation-Tolerant Ferroelectric Neural Computing: Special Session Paper". In: *2025 IEEE 68th International Midwest Symposium on Circuits and Systems (MWSCAS)*. IEEE. 2025, pp. 583–587.

[4] Tao Zhang, Mingjie Hu, **Md Zesun Ahmed Mia**, Hao Zhang, Wei Mao, Katsuyuki Fukutani, Hiroyuki Matsuzaki, Lingzhi Wen, Cong Wang, Hongbo Zhao, et al. "Self-sensitizable neuromorphic device based on adaptive hydrogen gradient". In: *Matter* 7.5 (2024), pp. 1799–1816.

Recognitions

- Melvin P. Bloom Memorial Outstanding Doctoral Research Award (2026)
- The Wormley Family Graduate Fellowship, Harry G. Miller Fellowships in Engineering (2025)
- Arthur Waynick Graduate Scholarship (2024),Milton and Albertha Langdon Memorial Fellowship (2023), Melvin P. Bloom Memorial Fellowship (2022)

Professional Affiliations

- Reviewer, IEEE TNNLS (2025), Design Automation Conference (DAC) (2025), IEEE MWSCAS (2025)
- Student Member, IEEE (2015-Present), Executive Member, EDS, IEEE BD (2021-2022)

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