Study of 3-nm Cylindrical GAAFETs with Variations in High-k Dielectric Gate-oxide Materials

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Abstract— **Semiconductor devices using high k dielectric materials are widely adopted in memory and amplifier applications. Among the semiconductor devices gate all around-FET (GAAFET) is now the latest trend being used instead of other field effect transistors to serve the purpose of reducing the short channel effects (SCE). In this work, we examine the performance of a circular cross-section gate all around-field effect transistor (GAA-FET) with varying gate dielectric characteristics with high-k dielectric oxide materials (Al_2O_3, HfO_2, $HfSiO_4$, SiO_2, Ta_2O_5, TiO_2) across the 3-nm channel length. These simulations showed that even though the dielectric constant over the channel increases in value, both ION-IOFF ratio and transconductance upsurge. The obtained results indicated that raising the dielectric constant in a gate oxide reduces subthreshold slope (SS), increases amplification rate, and reduces threshold voltage (V_{TH}) roll-off as well. The Silvaco TCAD ATLAS simulation was calibrated against experimental data from different works of literature. The higher the dielectric constant, the lower the SCEs. It is also found that TiO2 is dominating over the other materials selected for the simulation for a higher value of dielectric constant.**

Keywords—high k dielectrics, SILVACO TCAD, GAAFET, cylindrical shaped

I. INTRODUCTION

To improve the speed of devices, reduce cost and make them more efficient the fundamental object, the transistor needs to be scaled down to quantum scale from the existing measurement and only then Moore's law [1] will persist. Reduction of channel length, use of high k dielectrics, using multi-gate FETs and beyond instead of classical gate structures can help in achieving quantum scale operations. Nevertheless, the impediments in this endeavor are the short channel effects (SCEs) during the quantum scaling [2]. The operation of such scaled transistors is disrupted [3] due to the SCEs. Due to this, additional applications have a variety of drawbacks, such as drain-induced barrier lowering (DIBL), which can have a significant negative impact. Moreover, threshold voltage roll-off, rise in leakage current, hot carrier effect, and velocity saturation have detrimental effects as well [4]. Due to an electrostatic decoupling between the source and drain, DIBL renders the gate ineffective. If the current on/off ratio is reduced, the transistor cannot be totally turned off or there may be other complications. [5]. All these consequences result from lowering the threshold voltage. When the gate length is shortened, the current drive is decreased, which results in a rise in the electric field strength within the drain and the source. The high magnitude of the electric field disrupts the proportional connection, which ultimately leads to velocity saturation and a drop in the current drive. If the channel length is reduced threshold voltage is lowered as well [6]. An increase in sub-threshold leakage current will eventually lead to an increase in the amount of power that is lost as heat. The primary factors that were discussed before contribute significantly to the poor performance of the planar structures. A variety of approaches have been explored in order to reduce the number of SCEs. One solution to this problem is to employ gate structures that are either multi-gate or modified. [7]. Several modified gates exist like SOI-FETs [8], double gate MOSFETs [9], Fin-FETs, triple gate [10], pi gate [11], omega gate [12], square gate GAAFETs [13], and cylindrical gate GAAFETs [14]. Double gate MOSFET [1] gives better electrostatic potential control than single gate MOSFET. Fin-FET gives better electrical control to lower leakage current and reduce SCEs as it becomes like a set of fins [11]. By 10-nm triple gate FETs give a high current driving capability as well as good gate control over the channel [15]. Pi gate structure improves electrostatic potential in the channel as the gate is grown into a buried oxide [16]. Omega gate is similar to GAA having good scaling down characteristics however it shows intense corner effects [17]. Square gate GAAFET lower the SCEs whereas it has corner effects as well [18]. Cylindrical GAAFET has outdone all previous gate structures having better electrostatic control and overcoming SCEs [7]. As a result, it is in a better position for scaling down the transistor and keeping Moore's law [1] sustained.

In this work, we have simulated several cylindrical-shaped GAAFETs using different gate oxide materials. The effects of the variation have been analyzed regarding the existing literature. Drain current vs. drain voltage, subthreshold slope (SS), transconductance (g_m), on and off current and their ratio is found in Silvaco TCAD. The effects are demonstrated using different graphical representations and tables. TiO2 is dominant compared to other materials. However, given the cost, HfO2 is frequently utilized. Finding a relatively inexpensive material with adequate qualities will be a future focus of this research. To modify the transistor characteristics, physical factors like channel radius and oxide thickness including the oxide materials will be taken into account.

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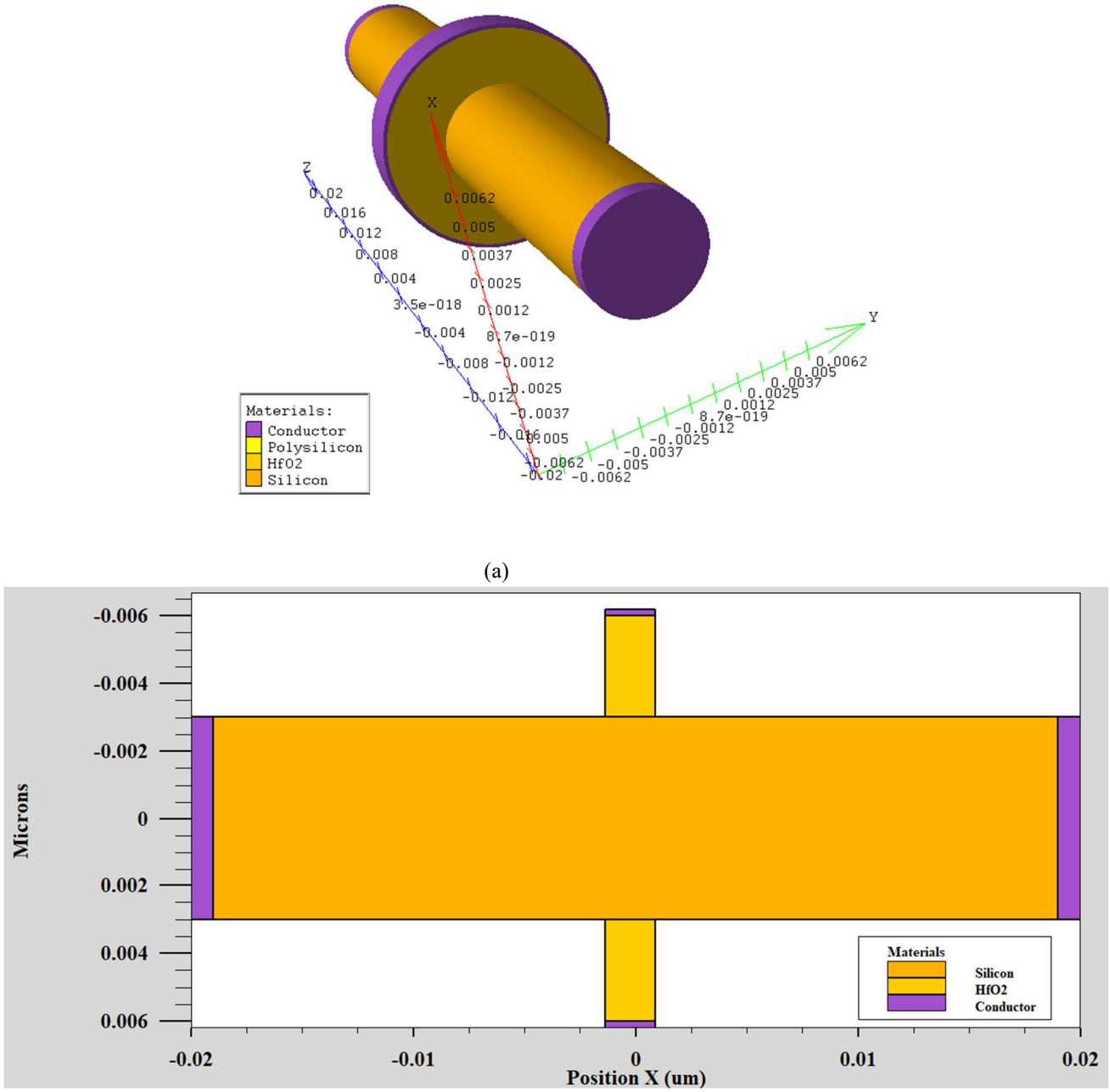

(a)

(b)

Fig.1 (a) 3nm Si-based GAAFET
(b) Cross-sectional representation of different regions of 3nm Si-based GAAFET

II. Device Structure and Simulation

A. Device structures

Figures 1 show the simulated device structures and doping profiles of various regions of Silicon (Si) based 3nm gate all around Field Effect Transistor (GAAFET). This is the basic structure simulated in this paper. Several oxide materials with increasing dielectric constants are used to vary. The structures are simulated using the corresponding parameters listed in table 2 from section B.

Table 1 [19] shows the static dielectric constants of materials used as gate oxides. Six oxide materials are chosen to simulate using existing literature [19]. The materials are varied while keeping the parameters from table 2 fixed to complete the simulation.

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Our developed device is simulated using Silvaco TCAD Altas. Design specifications for the 3D cylindrical 3nm-GAAFET include a 3nm channel length (L_g), a 2nm channel radius (R_c), and a 3nm oxide thickness (t_{ox}). With a doping density of 1×10^{20} atoms/cm3, channel doping is done using concentrations of P-type doping. Once more, drain and source doping concentrations of 1×10^{16} atoms/cm^3 are carried out using N-type doping concentrations. A 0.8 volt supply drain voltage and a 1-volt gate voltage are used.

B. Parameter tables

Table 1 Oxide materials used in structures

Oxide Materials	**Di-Electric Constant (static)**	**C_{ox} = Di-Electric Constant/t_{ox}**
Al_2O_3	9	3
HfO_2	25	8.33
$HfSiO_4$	11	3.67
SiO_2	3.9	1.3
Ta_2O_5	22	7.33
TiO_2	80	26.67

Table 2 Parameters for designing 3nm Si-based GAAFETs for various gate-oxide materials comparison

Design Parameters	**Values**
Channel Length, L_g	3nm
Channel Radius, R_c	2nm
Oxide Thickness, t_{ox}	3nm
Channel Doping Concentration, (P – type)	1×10^{20} atoms/ cm^3
Drain / Source Doping Concentration, (N-type)	1×10^{16} atoms/ cm^3
Drain Voltage	0.8 V
Gate Voltage	1 V

III. Result and Findings

In this section, a comparison of several dielectric materials used as the gate oxide of a cylindrical GAAFET has been provided. The comparative results and their impacts are explored for a few applications.

A. Drain current characteristics

When the gate voltage is below the threshold voltage, the device is said to be in the "OFF state." Subthreshold current, which does not necessarily need to be in the "OFF state," is the current flow produced by the minority charge carriers. The ON current is started by the gate voltage, which is higher than the threshold voltage.

Drain current vs. drain voltage for different gate dielectric materials is shown in fig. 2. Fig. 3 shows the drain current of GAAFET for SiO_2, Al_2O_3, HfO_2, $HfSiO_4$, Ta_2O_5, and TiO_2 against gate-to-source voltages. From fig. 4 it can be observed that for HfO_2, TiO_2, and Ta_2O_5 the leakage current is the same however for the rest of the dielectrics the leakage currents (OFF state current) are a little bit higher. With a low leakage current in SRAM applications, the signal-to-noise margin (SNM) increases. A better SNM might be obtained by employing high k dielectrics since their leakage current is lower.

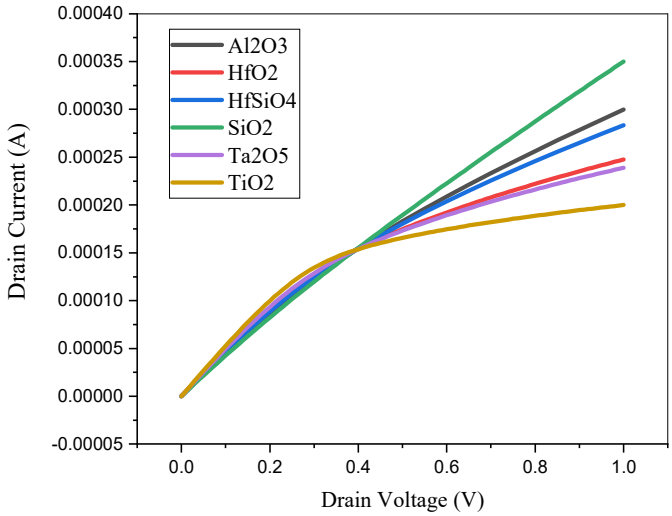

Fig.2 I_d vs V_{DS} curve for different gate oxide materials

When the gate voltage is applied in Fig. 4, the drain current, which is below the threshold voltage, also rises. The logarithmic scale is used for the I_d vs. V_{GS} displayed in Fig. 4. Thus, the increase in threshold voltage is seen. The drain current increases exponentially below the threshold voltage. The applied voltage of 0.7 V causes the current to stabilize. These changes may be compared using a subthreshold slope

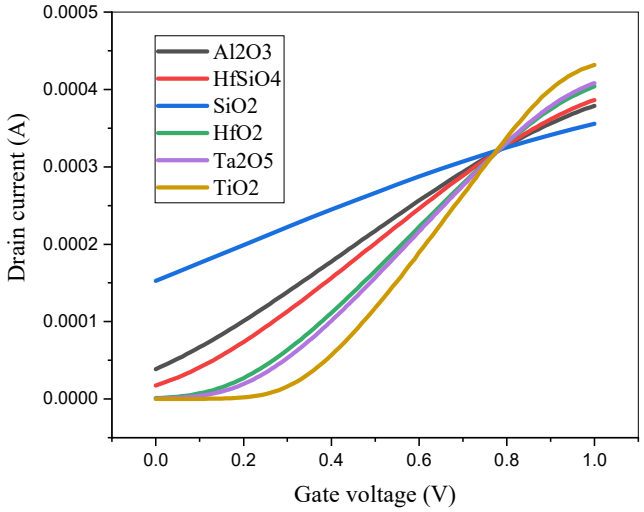

Fig.3 I_d vs V_{GS} curve for different gate oxide materials

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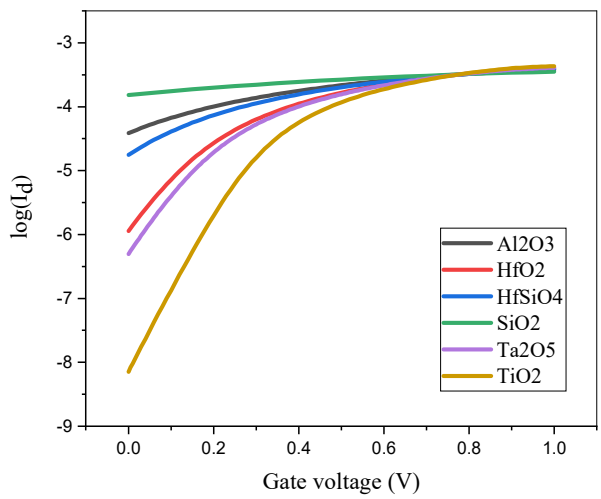

Fig.4 log (I_d) vs V_{GS} curve for different gate oxide materials

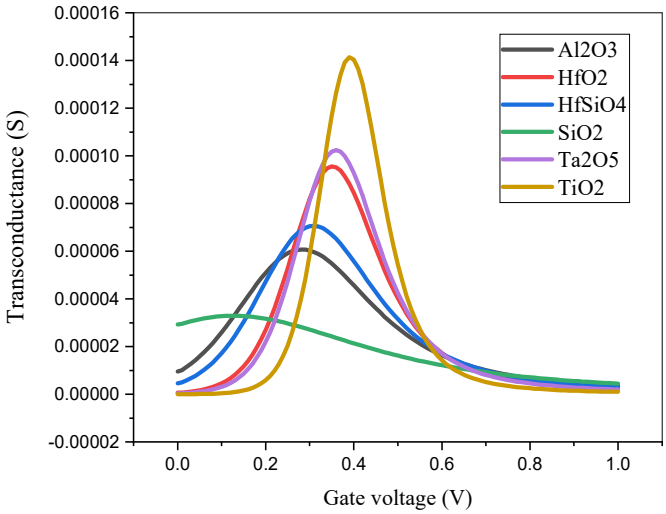

Fig.5 g_m vs V_{GS} curve for different gate oxide materials

B. Subthreshold parameters

Subthreshold slope (SS)

$$SS = [\frac{d(log10Id)}{dVG}]^{-1} \quad \text{.....(1)}$$

In the formula, VG = applied gate voltage and Id = resulting drain current

From table 3 we can observe that for TiO_2 the SS is lowest as the subthreshold voltage is low. For the other high k dielectrics, the characteristics of SS show a similar pattern as well. However, for Al_2O_3, SiO_2, and $HfSiO_4$ the SS is comparatively high. Low subthreshold swing decreases the dissipated heat in devices having short channel lengths [7] which adds to the superior characteristics of TiO_2, Ta_2O_5, and HfO_2.

Transconductance (g_m)

$$g_m = \frac{d(Id)}{dVDS} \quad \text{.....(2)}$$

In fig. 5 transconductance vs gate voltage curve is shown. Transconductance determines the amplification rate of any device means the amount of drain current impacted by gate voltage [20]. From fig. 5 it can be observed that the amplification rate of TiO_2 is the highest and the lowest is for SiO_2.

Table 3 shows that TiO_2 has the lowest OFF current while having the highest ON current. SiO_2 has a larger OFF current and a smaller ON current, on the other hand. TiO_2 has a larger I_{on}-I_{off} ratio than the other oxides as a result, whereas SiO_2 has the lowest ratio. SiO_2 has an on-to-off ratio that is almost ten times lower than Al_2O_3's. TiO_2 outperforms SiO_2 in the ratio by almost 10,000 times. The higher the I_{on}-I_{off} ratio the greater the gate control we can exercise [21]. Table 3 further demonstrates that materials with high k dielectric constants have greater gate control abilities.

Table 3 g_m vs V_{GS} curve for different gate oxide materials

Materials	Ion (A)	Ioff (A)	Ion/Ioff	SS
Al2O3	2.63×10-05	6.78×10-07	38.7387	0.18719
HfO2	2.74×10-05	2.59×10-08	1057.12	0.10726
HfSiO4	2.67×10-05	2.65×10-07	100.519	0.15131
SiO2	2.45×10-05	6.47×10-06	3.7905	0.58374
Ta2O5	2.76×10-05	1.42×10-08	1939.99	0.1005
TiO2	2.83×10-05	7.32×10-10	38681.2	0.078245

IV. CONCLUSION

This paper investigates the effect of variation in gate oxide materials for cylindrical-shaped gate all around FET using the gate length of 3 nm, oxide thickness of 2 nm, and channel radius of 2 nm. A higher on current is found with a higher dielectric constant as well as a lower off current is found with the higher dielectric constant. TiO_2 with the above combination is showing a higher drain current and high transconductance. Therefore devices having a higher dielectric constant in the oxide materials present superior features than the lower dielectrics as such higher on current, lower leakage current, higher amplification rate, and higher gate control ability. However, while having improved properties, materials with a higher dielectric constant are not cost-effective. The goal of this study in the future is to find a superior material with suitable qualities that is also affordable. Other physical characteristics will be considered in order to identify the right material and accomplish the required attributes. The factors that will be adjusted to achieve the aim are channel radius and oxide thickness.

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